Express Mail Label EV 099149623 US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	YONGSAM MOON *ET AL.*	EXAMINER:	UNKNOWN
APPLICATION NO.:	TO BE ASSIGNED	ART UNIT:	UNKNOWN
FILED:	HEREWITH	CONF. NO:	UNKNOWN
FOR:	**WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP**		

Information Disclosure Statement Within Three Months of Application Filing or Before First Action – 37 C.F.R. § 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. Timing of Submission

This information disclosure is being filed within three months of the filing date of this application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever occurs last [37 C.F.R. § 1.97(b)]. The references listed on the enclosed Form PTO-1449 (modified) may be material to the examination of this application; the Examiner is requested to make them of record in the application.

2. Cited Information

☒ Copies of the following references are enclosed:

- ☒ All cited references listed on PTO 1449 Form enclosed
- ☐ References marked by asterisks
- ☐ The following:

☐ Copies of the following references can be found in parent U.S. Application No. :

- ☐ All cited references
- ☐ References marked by asterisks
- ☐ The following:

☐ This application was filed after 30 June 2003 and no copies of U.S. patents nor published applications are enclosed (See Notice of Deputy Commissioner Kunin on 11 July 2003).

☐ The following references are not in English. For each such reference, the undersigned has enclosed (i) a translation of the reference; (ii) a copy of a communication from a foreign patent office or International Searching Authority citing the reference, (iii) a copy of a reference which appears to be an English-language counterpart, or (iv) an English-language abstract for the reference prepared by a third party. Applicant has not verified that the translation, English-language counterpart or third-party abstract is an accurate representation of the teachings of the non-English reference, though, and reserves the right to demonstrate otherwise.

- ☐ All cited references
- ☐ References marked by ampersands
- ☐ The following:

3. Effect of Information Disclosure Statement (37 C.F.R. § 1.97(h))

This Information Disclosure Statement is not to be construed as a representation that: (i) a search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the cited information is, or is considered to be, material to patentability. In addition, applicant does not admit that any enclosed item of information constitutes prior art to the subject invention and specifically reserves the right to demonstrate that any such reference is not prior art.

4. Fee Payment

No fees are believed due because this Information Disclosure Statement is being filed before the mailing date of the first Office Action.

☒ Applicant further submits that no fee is due in light of the following certification under 37 C.F.R. § 1.97(e) (check only one):

- ☐ In accordance with 37 C.F.R. § 1.97(e)(1), the undersigned hereby states that each item of information submitted herewith was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement; or

- ☒ In accordance with 37 C.F.R. § 1.97(e)(2), the undersigned hereby states that no item of information submitted herewith was cited in a communication from a foreign patent office in a counterpart foreign application, or, to the knowledge of the person signing the

certification after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c), more than three months prior to the filing of this statement.

However, should the Commissioner determine that fees are due in order for this Information Disclosure Statement to be considered, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 50-2207.

5. Patent Term Adjustment (37 C.F.R. § 1.704(d))

☐ The undersigned states that each item of information submitted herewith was cited in a communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this statement. 37 C.F.R. § 1.704(d).

Respectfully submitted,
Perkins Coie LLP

Date: November 25, 2003

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Form PTO-1449 (Modified) (Use several sheets if necessary)				COMPLETE IF KNOWN	
				Application Number	To be assigned
				Express Mail Label No.:	EV 099149623 US
				Filing Date	Herewith
				First Named Inventor	Yongsam Moon et al.
Sheet	1	of	2	Attorney Docket No.	59472-8086.US04

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.	U.S. Patent or Application NUMBER	Kind Code (if known)	Name of Patentee or Inventor of Cited Document	Date of Publication or Filing Date of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

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OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

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	A	Lee, C. Yoo, W. Kim, S. Chai, and W. Song, "A 622Mb/s CMOS Clock Recovery PLL with Time-Interleaved Phas Detector Array," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 198-199.	
	B	Fiedler, R. Mactaggart, J. Welch, and S. Krishnan, "A 1.0625 Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis," in *IEEE ISSC Dig. Tech. Papers*, Feb. 1997, pp. 238-239.	
	C	R. Gu, J. M. Tran, H.-C. Lin, A.-L. Yee, and M. Izzard, "A 0.5 – 3.5Gb/s Low-Power Low-Jitter Serial Data CMOS Transceiver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 352-353.	
	D	T. H. Lee, K. S. Donnelly, J. T. C. Ho, J. Zerbe, M. G. Johnson, and T. Ishikawa, "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," *IEEE J. Solid-State Circuits*, Vol. 29 (12/1994), pp. 1491-1496.	
	E	Efendovich, Y. Afek, C. Sella, and Z Bikowsky, "Multifrequency Zero-Jitter Delay-Locked Loop," *IEEE J. Solid-State Circuits*, Vol. 29, No. 1 (1/1994), pp. 26-70.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application(s).

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				Application Number	To be assigned
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				First Named Inventor	Yongsam Moon et al.
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	F	S. Sidiropoulos, and M. A. Horowitz, "A Semi-Digital Dual Delay-Locked Loop," *IEEE J. Solid-State Circuits*, Vol. 32, No. 11, (11/1997), pp. 1683-1692.	
	G	Y. Moon, J. Choi, K. Lee, D.-K. Jeong, and M.-K Kim, "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance," *IEEE J. Solid-State circuits*, Vol. 35, (3/2000), pp. 377-384.	
	H	Ian A. Young, J. K. Greason, and K. L. Wong, "A PLL Clock generator with 5 to 100 MHz of Lock Range for Microprocessors", *IEEE Journal of Solid-State Circuits*, Vol. SC-27, (11/1992), pp. 1599-1607.	

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